AF/2818 JFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Simon J. Lovett et al.	§	Group Art Unit: 2818
Serial No.: 09/942,898	§	Examiner: Pham, Ly D.
Filed: August 30, 2001	§	
For: ZERO POWER CHIP STANDBY MODE	§	Atty Docket: MICS:0071/FLE 00-0901

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June 25, 2004 — Maria Galloway
Date — *Maria Galloway*

Sir:

APPEAL BRIEF PURSUANT TO 37 C.F.R. §§ 1.191 AND 1.192

This Appeal Brief is being filed in furtherance to the Notice of Appeal mailed on April 22, 2004, and received by the Patent Office on April 26, 2004.

As a preliminary matter, in the Final Official Action mailed Janurary 22, 2004, the Examiner rejected claims 1-12 under 35 U.S.C. § 103(a) as being unpatentable over the combination of the McAdams and Weaver references. Subsequently, the Examiner rejected claims 7 and 12 under 35 U.S.C. § 103(a) as being unpatentable over the combination of the McAdams, Weaver, and Hoffman references. Appellants believe that the Examiner did not intend to reject claims 7 and 12 under the McAdams and Weaver references, because in the detailed discussion of the rejection, the Examiner only discussed the references as applied to

claims 1-6 and 8-11. Further, the Examiner admitted in the rejection of claims 7 and 12 that the McAdams and Weaver references failed to disclose various features recited in claims 7 and 12. Accordingly, Appellants have addressed the rejections based on the assumption that the Examiner intended to reject only claims 1-6 and 8-11 based on the McAdams and Weaver references alone.

1. REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc., the Assignee of the above-referenced application by virtue of the Assignment recorded at reel 012154, frame 0605, and dated August 30, 2001. The Assignee of the above-referenced application, as evidenced by the documents mentioned above, will be directly affected by the Board's decision in the pending appeal.

2. RELATED APPEALS AND INTERFERENCES

Appellants are aware of the Appeal of a divisional application (U.S. Patent Application No. 10/232,935). The undersigned is Appellants legal representative in this Appeal. Micron Technology, Inc., the assignee of the above-referenced application, as evidenced by the documents mentioned above, will be directly affected by the Board's decision in the pending appeal.

3. STATUS OF CLAIMS

Claims 1-12 are currently pending, and claims 1-12 are currently under final rejection, and thus, are the subject of this appeal.

4. STATUS OF AMENDMENTS

All amendments made to the claims have been entered. No amendments have been made since the Final Official Action was mailed on January 22, 2004.

5. SUMMARY OF THE INVENTION AND OF THE DISCLOSED EMBODIMENTS

The present application relates to a "zero-power" standby mode for a memory device. *See* Application, page 2, lines 7-11. In wireless, battery-powered handheld device, an operating system utilizes various software programs to provide computing functions to the user. *See id.* at page 2, line 25 to page 3, line 5. Often, these wireless, battery-powered handheld devices utilize techniques to reduce power consumption without reducing device functionality by providing a low power mode to extend battery usage. *See id.* at page 3, lines 16-25. Accordingly, a zero-power standby mode may be implemented to minimize current and power consumed by the system. *See id.* Despite these efforts, standby modes typically result in leakage currents of ten to twenty micro amps from complimentary metal-oxide-semiconductor (CMOS) technology, which is typically used in Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) devices. *See id.* at page 3, lines 26-32.

The present technique reduces the leakage current to provide a true zero-power standby mode for increasing battery life for handheld devices. To prevent or further reduce the leakage currents in the standby mode, an isolation circuit, such as a p-channel field effect transistor (FET) 28, may be utilized to disconnect the CMOS inverter 27 on the SRAM/DRAM chip from a power signal Vcc delivered by an external power supply 14. *See id.* at page 6, line 25 to page 7,

line 13. The p-channel FET 28 is inserted in the path of the voltage signal Vcc to eliminate the junction leakage. *See id.* at page 8, lines 30-32.

The p-channel FET 28 receives a control signal POWERDOWN on a gate 58 to control the isolation circuit. *See id.* at page 9, lines 7-10. Based on the state of the control signal POWERDOWN, all internal voltage signals Vccx from an internal power supply bus 60 will be isolated completely from or coupled to the external power signal Vcc through the isolation circuit (e.g. FET 28). *See id.* at page 9, lines 11-22. In a normal mode of operation, the control signal POWERDOWN is disabled, and the external voltage signal Vcc is delivered to the internal power bus 60 via a pad 66. *See id.* at page 10, line 14 to page 11, line 1. In the standby mode, the control signal POWERDOWN is enabled, which isolates the power signal Vcc from the internal power bus 60. *See id.* at page 11, lines 2-10. As a result, leakage current from CMOS memory device, such as the SRAM/DRAM chip 64, is eliminated and true zero-power standby mode is achieved. *See id.* Thus, the p-channel FET 28 acts as a master switch to disconnect the external power signal Vcc from the internal power bus 60 inside the DRAM/SRAM or other semiconductor device.

6. ISSUES

Issue No. 1:

Whether claims 1-6 and 8-11 are unpatentable under 35 U.S.C.§ 103(a) as being rendered obvious by McAdams (U.S. Patent No. 5,301,160) in view of Weaver et al. (U.S. Patent No. 4,107,596).

Issue No. 2:

Whether claims 7 and 12 are unpatentable under 35 U.S.C.§ 103(a) as being rendered obvious by McAdams (U.S. Patent No. 5,301,160) in view of Weaver et al. (U.S. Patent No. 4,107,596) and Hoffman et al. (U.S. Patent No. 5,117,129).

7. GROUPING OF CLAIMS

In regard to Issue No. 1, independent claim 1 will stand or fall separately and dependent claims 2-6 and 8-11 will stand or fall with independent claim 1.

In regard to Issue No. 2, claims 7 and 12 will stand with independent claim 1, but will fall separately.

8. ARGUMENT

As discussed in detail below, the Examiner has improperly rejected the pending claims. Further, the Examiner has misapplied long-standing and binding legal precedents and principles in rejecting the claims under Section 103. Accordingly, Appellants respectfully request full and favorable consideration by the Board, as Appellants strongly believe that claims 1-12 are currently in condition for allowance.

Issue No. 1:

The Examiner rejected claims 1-6 and 8-11 under 35 U.S.C.§ 103(a) as being unpatentable over McAdams (U.S. Patent No. 5,301,160) in view of Weaver et al. (U.S. Patent No. 4,107,596). Specifically, with regard to independent claim 1, the Examiner stated:

> Regarding **claim 1**, McAdams discloses a system comprising: a processor (fig. 1, 102), a power supply coupled to the processor (fig. 1, 112); and a device coupled to the processor and the power supply and comprising (fig. 2): an internal power supply bus configured to receive a power signal from the power supply (fig. 2, buses internal to 145 supplying Vdd 112); and an isolation circuit configured to disconnect the internal power supply bus from the power supply bus by interrupting the flow of the power signal (fig. 2, isolating circuit being p-mos transistors 282 and 284, which are configured to interrupt the power signals to TL and TR lines, which feed power to the memory section, right dotted box in fig. 2).
>
> Although McAdams did not explicitly show the isolation circuit receives a control signal to interrupt the flow of power during a standby mode; however practice of such feature, in which standby signal which control the isolation circuit to isolate the power from the load, is considered well known in the art. An exemplary instance is shown by Weaver et al. (col. 10, lines 57-60, '...OFF high impedance state for the duration of the standby mode in response to the standby-operate signal for isolating the load from the battery...').
>
> Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the teaching by Weaver to the disclosure of McAdams so that minimal control current during standby mode (col. 1, lines 35-42).
> Final Official Action mailed January 22, 2004, page 2-3.

Appellants respectfully traverse this rejection. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination or modification. *See ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been

obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination or modification to render obvious a subsequent invention, there must be some reason for the combination or modification other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination or modification. *See Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

The present application is directed to a technique for implementing a zero-power standby mode with reduced leakage current, as discussed above. To implement the zero-power standby mode, an isolation circuit is utilized within a memory device. The isolation circuit, which is activated by a control signal, disconnects an internal power supply bus from an external voltage source to reduce leakage currents in response to initiating a standby mode. *See id.* at page 9, lines 3-9; page 9, lines 15-27; page 10, line 25 – page 11, line 7. Specifically, claim 1 recites "an isolation circuit configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal when a standby mode is indicated by a control signal received at the isolation circuit."

In contrast to the claimed subject matter, McAdams describes a selection circuit that enables transmission through transfer gates in response to address signals. *See* McAdams, col. 2, lines 9-18 and 31-32. The selection circuit provides either precharged voltage to the transfer gates or a high level signal to one of the transfer gates when selecting a transfer gate. *See id.* at col. 2, lines 33-36. In the McAdams reference, a bitline isolation control circuit 145 includes two

voltage supply selection circuits that are controlled by signals produced from the row address decoder 124. *See id.* at Fig. 2; col. 5, lines 15-17. The bitline isolation control circuit 145 switches between a precharged state from off-chip voltage supply Vdd and an active state from on-chip voltage supply Vpp. *See id.* at col. 5, lines 40-51. The selection between these voltage sources is based on row address select signals RA8 and $\overline{RA8}$ along with row address selection signals RA9 and $\overline{RA9}$, which are applied to the inputs of the bitline isolation control circuit 145. *See id.* at col. 5, lines 26-33 and 46-51. Thus, McAdams describes providing one of two voltage signals based upon address signals received at the bitline isolation control circuit 145.

The Weaver reference is directed to a bidirectional DC-to-DC power converter. *See* Weaver et al., col. 1, lines 7-10. In the Weaver reference, a hand-held unit 110 is divided into a control module 130 and power module 140. *See id.* at Fig. 1; col. 2, lines 29-32. The power module 140 contains a power source 142 and a power control logic 144 that provide a standby voltage (SBY) during a low power standby mode when the control model 130 is not active. *See id.* at col. 2, lines 37-43. During an operate mode the power source 142 applies an operate voltage V_{OPR} to activate data flow and control circuits. *See id.* at col. 2, lines 43-47. The power source 142 includes a power supply 220 along with a battery 204. *See id.* at Fig. 2; col. 2, lines 62-67; col. 3, lines 14-32. This power supply 220 includes transistors Q1, Q2 and Q3 that operate with a ramp generator 516 and a feedback amplifier 520. *See id.* at Fig. 5; col. 7, line 20-col. 8, line 43. As such, the bidirectional power converter of the Weaver reference is a portion of the power supply or power converter 220.

In the rejection of independent claim 1, the Examiner stated that the McAdams reference discloses all of the claimed subject matter except that "the isolation circuit receives a control signal to interrupt the flow of power during standby mode." Specifically, in the rejection, the Examiner asserted that the bitline isolation control circuit 145 of McAdams is equivalent to the "device" recited in claim 1, that the enhancement mode MOS transistors 282 and 284 of McAdams are equivalent to the "isolation circuit" recited in claim 1, and that the transfer control leads TR and TL of McAdams are equivalent to the "internal power supply bus" recited in claim 1. In an attempt to cure this deficiency of "the isolation circuit receives a control signal to interrupt the flow of power during standby mode," which is not disclosed in the McAdams reference, the Examiner relied upon the Weaver reference to disclose this recited feature.

Despite the Examiner's assertions, however, Appellants respectfully assert that the McAdams and Weaver references, alone or in combination, fail to render the claimed subject matter obvious for at least two reasons. First, the references fail to disclose "an isolation circuit configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal when a standby mode is indicated by a control signal received at the isolation circuit," as recited in claim 1. Secondly, the Examiner has failed to provide a convincing line of reasoning as to why one of ordinary skill in the art would have found any motivation or suggestion to make such a combination. Hence, the McAdams and Weaver references fail to render the claimed subject matter obvious.

With regard to the first point, the McAdams and Weaver references fail to disclose "an isolation circuit configured to disconnect the internal power supply bus from the power supply by

interrupting the flow of the power signal when a standby mode is indicated by a control signal received at the isolation circuit," as recited in independent claim 1. As noted above, the Examiner asserted that the bitline isolation control circuit 145 of McAdams is equivalent to the "device" in claim 1, that the enhancement mode MOS transistors 282 and 284 of McAdams are equivalent to the "isolation circuit" of claim 1, and that the transfer control leads TR and TL of McAdams are equivalent to the "internal power supply bus" of claim 1. Also, the Examiner admitted that the McAdams reference does not "explicitly show that the isolation circuit receives a control signal to interrupt the flow of power during a standby mode."

With regard to the McAdams reference, the row address select and selection signals RA8, RA9, $\overline{RA8}$ and $\overline{RA9}$ are used by the bitline isolation circuit 145 to select between two voltage supplies that are provided to the transfer control leads TR and TL. *See* McAdams, col. 5, lines 26-32. The McAdams reference clearly describes that the voltage supply selection circuits are controlled by the signals produced from the row address decoder 124, and are not *a control signal that indicates a standby mode*. *See* McAdams, col. 5, lines 15-17. In fact, the row address select and selection signals RA8, RA9, $\overline{RA8}$ and $\overline{RA9}$ are specifically described as providing access to specific bitlines in the memory array 110 for the sense amplifier 200 through the transfer control leads TR and TL. *See* McAdams, col. 5, lines 21-32. Clearly, nothing in the reference suggests or teaches that the enhancement mode MOS transistors 282 and 284 are controlled by a signal indicating a standby mode. Accordingly, the McAdams reference does not disclose or teach the claimed subject matter.

To cure the deficiencies of the McAdams reference, the Examiner relied upon a passage at col. 10, lines 57-60, of the Weaver reference. However, the cited reference fails to cure the deficiencies of the McAdams reference. In the cited passage of the Weaver reference, a controlled output switching means is a part of a bidirectional power converter. *See* Weaver et al., col. 10, lines 20-64. As noted above, the power converter is described in the reference as the power source or converter 220. *See* Weaver et al., col. 6, lines 62-67. The power converter 220 is part of (i.e. internal to) the power supply, and the Weaver reference merely discloses disabling the supply of power from the power supply to other components of the system that are external to the power supply. Clearly, it does not disclose *an isolation circuit in a device coupled to the power supply and a processor*, which is "configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal when a standby mode is indicated by a control signal received at the isolation circuit," as recited in claim 1. Accordingly, the Weaver reference does not cure the deficiencies of the McAdams reference. As such, because the Weaver reference and the McAdams reference, alone or in combination, fail to disclose or suggest all the recited features, the cited references fail to render the claimed subject matter obvious.

With regard to the second point, to provide support for the proposed combination of the references, the Examiner merely stated:

> Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the teaching by Weaver to the disclosure of McAdams so that minimal control current during standby mode (col. 1, lines 35-42). Final Official Action mailed January 22, 2004, page 3.

The Examiner's statement is not a convincing line of reasoning at to *why* one of skill in the art would combine the references, but is an unsupported assertion, which does not meet the evidentiary standard required for combining references under Section 103.

Specifically, the McAdams and Weaver references simply do not provide a suggestion or motivation for the asserted combination. In the McAdams reference, as noted above, row address select and selection signals RA8, RA9, $\overline{RA8}$ and $\overline{RA9}$ are used by the bitline isolation circuit 145 to select between two voltage supplies that are supplied to the transfer control leads TR and TL. *See* McAdams, col. 5, lines 26-32. The McAdams reference clearly describes that the voltage supply selection circuits are controlled by the signals produced from the row address decoder 124. *See* McAdams, col. 5, lines 15-17. The McAdams reference clearly provides one voltage or another based on the address signals, and is not even associated with a standby mode. In contrast to the McAdams reference, the Weaver reference is not concerned with address signals or providing access to a memory array because the reference is directed to DC-to-DC power converters. Indeed, the reference describes a power converter that may be changed with minimal control current and functions in a standby mode and an operation mode. *See* Weaver et al., col. 1, lines 34-42. As such, the references simply do not provide a suggestion or motivation for the proposed combination.

Because the Examiner has failed to show that the cited references disclose *all* of the claimed elements, much less provide a convincing line of reasoning as to why one of ordinary skill in the art would have found the claimed invention obvious in light of the cited references, the Examiner has failed to establish a *prima facie* case of obviousness. For at least these reasons,

Appellants request that the Board reverse the Examiner's rejection of independent claim 1 and dependent claims 2-6 and 8-11.

Issue No. 2:

The Examiner rejected claims 7 and 12 under 35. U.S.C. § 103(a) as being unpatentable over McAdams (U.S. Pat. No. 5,301,160) in view of Weaver et al. (U.S. Patent No. 4,107,596) and Hoffman et al. (U.S. Pat. No. 5,117,129). Appellants respectfully traverse this rejection.

In the rejection of claims 7 and 12, the Examiner asserted that the McAdams and Weaver references disclose all of the recited features except the isolation circuit coupled between a pad on the device configured to receive the power signal and the internal power supply bus, and an I/O pad and circuitry coupled between the output buffer and the I/O pad to tri-state the I/O pad. *See* Final Office Action mailed on January 22, 2004, page 4. In an attempt to cure these deficiencies, the Examiner relied upon the Hoffman reference.

However, despite the Examiner's assertions, the McAdams, Weaver, and Hoffman references fail to render the claimed subject matter obvious for at least three reasons. First, the Hoffman reference does not cure the deficiencies of the McAdams and Weaver references with regard to independent claim 1, as discussed above with reference to Issue No. 1. Secondly, the references do not disclose or teach all of the additionally recited features of claims 7 and 12. For instance, the references do not disclose or suggest "wherein the isolation circuit is coupled between a pad on the device configured to receive the power

signal and the internal power supply bus," as recited in claim 7, and "circuitry coupled between the output buffer and the input/output pad and configured to tri-state the input/output pad," as recited in claim 12. Thirdly, the Examiner's proposed suggestion or motivation to combine these references is not sufficient and, in fact, is not supported by the references. Hence, Appellants contend that the combination of the McAdams, Weaver, and Hoffman references fail to render the claimed subject matter obvious, as discussed further below.

With regard to the first point, claims 7 and 12 depend from independent claim 1 and are believed to be patentable based on this dependency. The Hoffman reference is directed to cold sparing of a full rail logic swing CMOS off-chip driver that presents high impedance to ground when power is not present. *See* Hoffman, col. 1, lines 36-39. Specifically, the reference describes a CMOS circuit that presents high impedance when the voltage V_{DD} is equal to ground. *See* Hoffman, col. 3, lines 1-5 and 37-56. In the Hoffman reference, the pad signal 150 is coupled to the I/O pad 152 through a circuit, which includes various transistors and logic devices. *See* Hoffman, Fig. 3A, col. 3, lines 25-30. The circuit, which the Examiner appears to assert is equivalent to the isolation circuit, is not even coupled to an *internal power supply bus,* as recited in the present claims. Further, the operation of the circuit is not based on a *control signal that indicates a standby-mode*, but rather is based on the voltage V_{DD}. *See*, Hoffman, col. 3, lines 36-56. Clearly, the Hoffman reference does not disclose an *isolation circuit* that disconnects *internal power supply bus* in response to a *control signal that indicates a standby mode*. As such, the Hoffman reference fails to cure the deficiencies of the McAdams and Weaver references.

With regard to the second point, the references do not disclose or teach that "the isolation circuit is coupled between a pad on the device configured to receive the power signal and the internal power supply bus," as recited in claim 7, or "circuitry coupled between the output buffer and the input/output pad and configured to tri-state the input/output pad," as recited in claim 12. As noted above, the Examiner admitted that the McAdams and the Weaver references fail to disclose an isolation circuit coupled between a pad on the device configured to receive the power signal and the internal power supply bus, and an I/O pad and circuitry coupled between the output buffer and the I/O pad to tri-state the I/O pad. However, contrary to the Examiner's assertions, the Hoffman reference fails to cure these deficiencies. As noted above, the Hoffman reference describes a CMOS circuit that presents high impedance when the voltage V_{DD} is equal to ground. *See* Hoffman, col. 3, lines 1-5 and 37-56. The pad signal 150 of Hoffman is coupled to the I/O pad 152 through a circuit, which includes various transistors and logic devices. *See* Hoffman, Fig. 3A, col. 3, lines 25-30. This circuit, which the Examiner appears to assert is equivalent to the isolation circuit, is not coupled to an *internal power supply bus,* much less, configured to *tri-state the input/output pad.* Accordingly, the Hoffman reference does not disclose the subject matter recited in claims 7 and 12.

With regard to the third point, to provide support for the proposed combination of the references, the Examiner merely stated:

> Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to include the feature shown by Hoffman et al. to the disclosure of McAdams to provide stable drive to loads, col. 2, lines 30-38.) Final Official Action mailed January 22, 2004, page 4.

The Examiner's statement is not a convincing line of reasoning at to *why* one of skill in the art would combine the references, but is an unsupported assertion does not meet the evidentiary standard required for combining references under Section 103 and is, in fact, unsupported by the references.

The McAdams, Weaver and Hoffman references simply do not provide a suggestion or motivation for the asserted combination. Indeed, the McAdams reference describes a bitline isolation control circuit 145 that is controlled by the signals produced from the row address decoder 124. The bitline isolation control circuit 145 provides one voltage or another based on the address signals, and is not even associated with a standby mode. In contrast, the Hoffman reference simply describes providing redundant circuits that are not powered. *See* Hoffman, col. 1, lines 14-22. Specifically, the Hoffman reference is directed to cold sparing of a full rail logic swing CMOS off-chip driver that presents high impedance to ground when power is not present. *See id.* at col. 1, lines 36-39. This inactive non-powered circuit is not useful in the McAdams reference, which relates to a selection circuit that provides one of two voltages to transfer gates. Thus, the references simply do not provide a suggestion or motivation for the asserted combination.

Further, while the Examiner does not rely upon the Weaver reference, it does not provide a suggestion or motivation for the asserted combination either. The Weaver reference describes a power converter that may be changed with minimal control current and functions in a standby mode and operation mode. *See* Weaver et al., col. 1, lines 34-42. In contrast, the Hoffman

reference simply describes providing redundant circuits, which do not leak current when they are not in use. Thus, the references simply do not provide a suggestion or motivation that would support the combination.

Because the Examiner has failed to show that the cited references disclose *all* of the claimed elements and fails to provide a convincing line of reasoning as to why one of ordinary skill in the art would have found the claimed invention obvious in light of the cited references, the Examiner has failed to establish a *prima facie* case of obviousness. For these reasons, Appellants requests that the Board reverse the rejection of the claims 7 and 12.

CONCLUSION

In view of the above remarks, Appellants respectfully submit that the Examiner has provided no supportable position or evidence that claims 1-12 are rendered obvious in view of the prior art. Accordingly, Appellants respectfully request that the Board find claims 1-12 patentable over the prior art of record and reverse all outstanding rejections.

The Commissioner is authorized to charge the requisite fee of $330.00, and any additional fees which may be required, to Deposit Account No. 13-3092; Order No. MICS:0071/FLE (00-0901).

General Authorization for Fees and Extensions of Time

In accordance with 37 C.F.R. § 1.136, Appellants request that this and any future reply requiring an extension of time be treated according to the General Authorization For Extensions

of Time previously submitted. Further, the Commissioner is authorized to charge the requisite fee of $330.00, and any additional fees which may be required, to Deposit Account No. 13-3092; Order No. MICS:0071/FLE (00-0901).

Respectfully submitted,

Date: June 25, 2004

Robert A. Manware
Reg. No. 48,758
FLETCHER YODER
P.O. Box 692289
Houston, TX 77269-2289
(281) 970-4545

9. **APPENDIX OF CLAIMS ON APPEAL**

1. A system comprising:

a processor;

a power supply coupled to the processor; and

a device coupled to the processor and the power supply and comprising:

an internal power supply bus configured to receive a power signal from the power supply; and

an isolation circuit configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal when a standby mode is indicated by a control signal received at the isolation circuit.

2. The system, as set forth in claim 1, wherein the system is a cellular phone.

3. The system, as set forth in claim 1, wherein the system is a personalized digital assistant (PDA).

4. The system, as set forth in claim 1, wherein the system is a handheld computer.

5. The system, as set forth in claim 1, wherein the device comprises a memory device.

6. The system, as set forth in claim 1, wherein the internal power supply bus is configured to provide the power signal to the device.

7. The system, as set forth in claim 1, wherein the isolation circuit is coupled between a pad on the device configured to receive the power signal and the internal power supply bus.

8. The system, as set forth in claim 1, comprising an input buffer comprising a control line configured to control the isolation circuit.

9. The system, as set forth in claim 8, wherein the isolation circuit comprises a p-channel field effect transistor (FET).

10. The system, as set forth in claim 9, wherein the gate of the p-channel FET is coupled to the control line of the input buffer.

11. The system, as set forth in claim 1, comprising an output buffer configured to buffer the device from the remainder of the system.

12. The system, as set forth in claim 11, comprising:

an input/output pad; and

circuitry coupled between the output buffer and the input/output pad and configured to tri-state the input/output pad.